



## Reduction of Total Harmonic Distortion in different level of NPCMLI multi level inverter with application of solar photovoltaic system

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**ABSTRACT:** Solar energy is the most promising member of renewable energy source. Photovoltaic cells convert solar energy into electrical energy in direct current form. Most of the applications are run through ac power. DC power converted into ac by using multilevel inverter. There are several ways to implement multilevel inverter like diode clamped, H-bridge and neutral point clamped multilevel inverter. Usually two-level inverters are mostly used to generate an AC voltage from an DC voltage. The two-level inverter can only create two different output or two level of voltages. But in case of two level inverter total harmonic distortion is not reduced because the output voltage waveform has only two level, in case of multilevel inverter these voltage levels extend so as to reduce THD. In this paper simulation of different level of multilevel inverter by using neutral point clamped topology presented to show as the level increases harmonic distortion level decreases. Simulation work is done using the MATLAB software and experimental results have been presented to validate the theory.

**Key words:** Multilevel inverter, NPC, PV cell, THD

### I. INTRODUCTION

#### A. Multilevel Inverter

For conversion of Direct current into alternating current inverter is used. In large power application total harmonic distortion increases considerably as the output voltage increase. In such type of applications conventional two level inverter is not suitable. In this condition utilization of multilevel inverter is comes under consideration. Several topologies are used for construction of multi level inverter. In cascade H bridge inverter topology the number of phase voltage levels at the converter terminals is  $2N+1$ , where N is the number of cells or dc link voltages. In this topology, each cell has separate dc link capacitor and the voltage across the capacitor might differ among the cells. So, each power circuit needs just one dc voltage source. The number of dc link capacitors is proportional to the number of phase voltage levels. Each H-bridge cell may have positive, negative or zero voltage. Final output voltage is the sum of all H-bridge cell voltages and is symmetric with respect to neutral point, so the number of voltage levels is odd.

Meynard and Foch introduced a flying-capacitor-based inverter in 1992 [1]. The structure of this inverter is similar to that of the diode-clamped inverter except that instead of using clamping diodes, the inverter uses capacitors in their place. This topology has a steps structure of dc side capacitors, where the voltage on

each capacitor differs from that of the next capacitor. The voltage increment between two adjacent capacitor legs gives the size of the voltage steps in the output waveform. One advantage of the flying-capacitor-based inverter is that it has redundancies for inner voltage levels; in other words, two or more valid switch combinations can synthesize an output voltage. Unlike the diode-clamped inverter, the flying-capacitor inverter does not require all of the switches that are on (conducting) be in a consecutive series. In addition to the  $(m-1)$  dc link capacitors, the m-level flying-capacitor multilevel inverter will require  $(m-1) \times (m-2)/2$  auxiliary capacitors per phase if the voltage rating of the capacitors is identical to that of the main switches. Besides the three basic multilevel inverter topologies previously discussed, Other multilevel converter topologies have been proposed; however, most of these are “hybrid” circuits that are combinations of two of the basic multilevel topologies or slight variations to them. Additionally, the combination of multilevel power converters can be designed to match with a specific application based on the basic topologies.

**Neutral point clamped multilevel inverter.** NPCMLI topology is used in this work, in this topology the use of voltage clamping diodes is vital. A common DC-bus is divided by a even number, which depend on the number of voltage levels in the inverter, of bulk capacitors in series with a neutral point in the middle of the line.

The reason for the inverter to have clamping diodes connected in series is so that all diodes can be of the same voltage rating and be able to block the right number of voltage levels.

The main concept of this inverter is to use diodes to limit the power devices voltage stress. The voltage over each capacitor and each switch is  $V_{dc}$ . Fig. 3. By increasing the number of voltage levels the quality of the output voltage is improved and the voltage

waveform becomes closer to sinusoidal waveform. Advantages of NPCMLI

- (i) When the number of levels is high enough, harmonic content will be low enough to avoid the need for filters.
- (ii) Efficiency is high due to all devices which are being switched at the fundamental frequency.

We are able to control the reactive power flow. The control method is easy for a back to back inverter system.

COMOPNENTS	NUMBERS
Levels	M
Switches and parallel diodes	2(m-1)
Capacitor	(m-1)
Clamping Diodes	(m-1)(m-2)

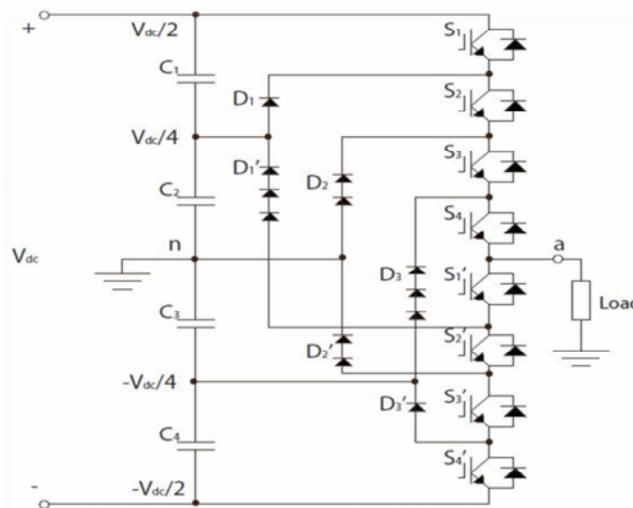


Fig. 1 Five-level NPC Inverter.

Operational function can be better understand in following five steps

- (i) For the output voltage,  $+\frac{V_{dc}}{2}$  switches  $S_1, S_2, S_3, S_4$  and are turned on.
- (ii) For the output voltage,  $+\frac{V_{dc}}{4}$  switches  $S_2, S_3, S_4$  and  $S_1'$  are turned on and the voltage is held by the help of the surrounding clamping diodes  $D_1$  and  $D_1'$ .
- (iii) For the output voltage zero switches  $S_3, S_4, S_1$  and  $S_2'$  are turned on and the voltage is held by the help of the surrounding clamping diodes  $D_2$  and  $D_2'$ .
- (iv) For the output voltage,  $-\frac{V_{dc}}{4}$  switches  $S_4, S_1', S_2'$  and  $S_3'$  are turned on and the voltage is held by the help of the surrounding clamping diodes  $D_3$  and  $D_3'$ .
- (v) For the output voltage,  $-\frac{V_{dc}}{2}$  switches  $S_1', S_2', S_3'$  and  $S_4'$  are turned on.

*B. Solar photovoltaic cell*

Photovoltaic systems act in an unusual and useful way: They react to light by transforming part of it into electricity solar PV system have no moving parts (in the classical mechanical sense) to wear out also it Contain no fluids or gases (except in hybrid systems) that can leak out, as do some solar-thermal systems so no need to fuel to operate The rapid offered by PV cell is rapid, achieving full output instantly can operate at fair temperatures Produce no pollution while producing electricity (although waste products from their manufacture, and toxic gases in the event of catastrophic failure and disposal may be a concern).

It Require little maintenance if properly manufactured and installed. It can be made from silicon, the second most abundant element in the earth's crust. Photovoltaic systems are capable of transforming one kilowatt of solar energy falling on one square meter into about a hundred watts of electricity.

Several methods are available for energy storage. The flywheel (a) is receiving considerable attention for PV and other systems, but proved systems are not yet commercially available. Pump-storage concepts (c) have been in mode for many years and are common among electric utilities seeking inexpensive peak-load reserve. (Air storage systems (b) are a variant of pumped hydro storage, being most suited to small-scale energy set-aside.) Batteries (d) are possibly the most common method for storing moderate amounts of DC power.

**C. Modulation**

arrival of the transformer less multilevel inverter topology has brought forth various pulse width modulation (PWM) schemes as a means to control the switching of the active devices in each of the multiple voltage levels in the inverter.

There are three alternative PWM strategies with different phase relationships:

- Alternate phase disposition (APOD) every carrier waveform is in out of phase with its neighbor carrier by  $180^{\circ}$ .
- Phase opposition disposition (POD) All carrier waveforms above zero reference are in phase

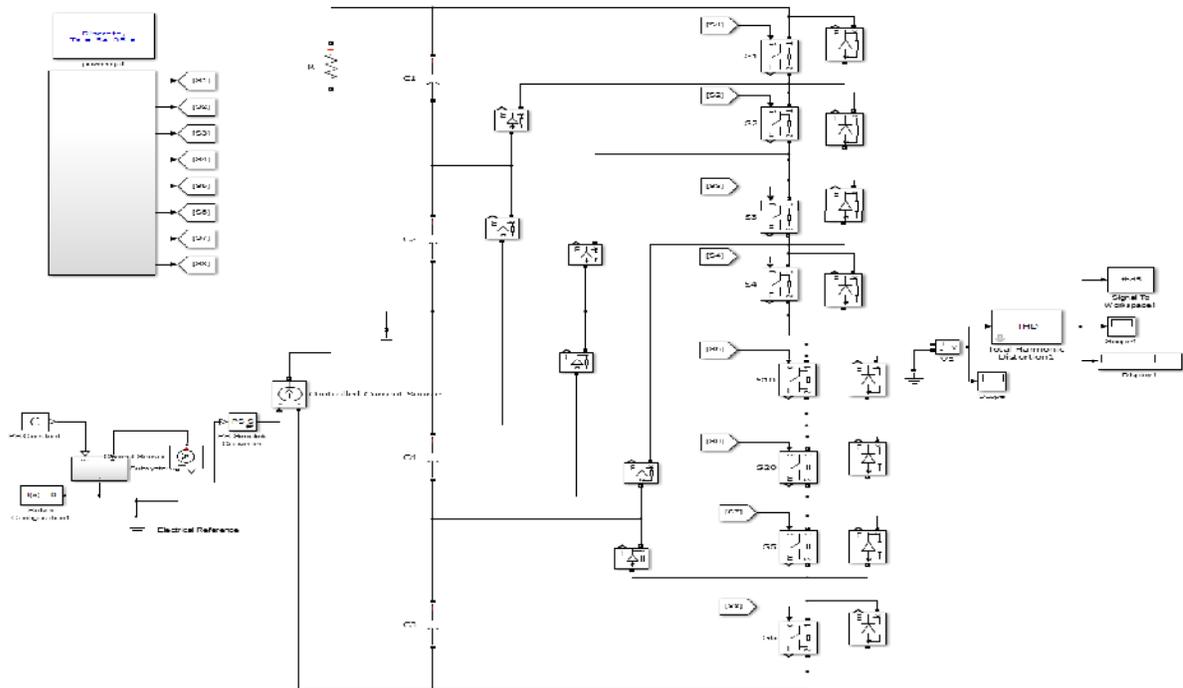
and are  $180^{\circ}$  out of phase with those below zero.

- Phase disposition (PD) All carrier waveforms are in phase.

For modulation of NPCMLI Phase opposition disposition is used. The rules for the phase opposition disposition method, when the number of level  $m = 7$ . The  $m - 1 = 6$  carrier waveforms are arranged so that all carrier waveforms above zero are in phase and are  $180^{\circ}$  out of phase with those below zero. The converter is switched to  $+V_{dc} / 2$  when the reference is greater than both carrier waveforms. The converter is switched to zero when the reference is greater than the lower carrier waveform but less than the upper carrier waveform.

**II. SIMULATION MODEL**

In Fig. 2 the simulation model of five Level Neutral Point Clamped Multilevel Inverter (NPCMLI) is presented. Sub system gives four switching pulses i.e.  $A_1, A_2, A_3, A_4, A_5, A_6, A_7$  and  $A_8$  for the switches  $S_1, S_2, S_3, S_4, S_5, S_6, S_7$  and  $S_8$  respectively. The switching pulses are set in such manner that the turning on and off should be same as the working principle of the Diode Clamped/Neutral Point Clamped Multilevel Inverter (NPCMLI).



**Fig. 2.** Simulation model of five level inverter.

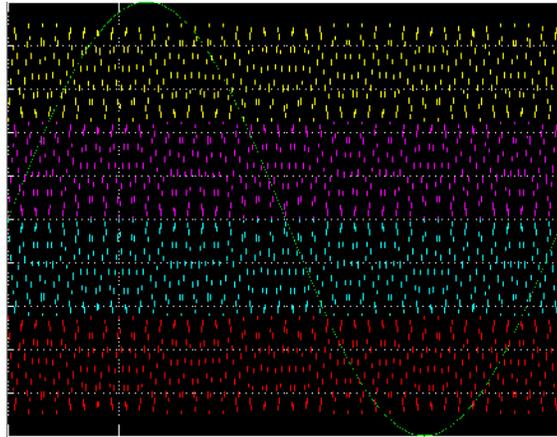


Fig. 3. Sine Pulse width modulation for five level inverter.

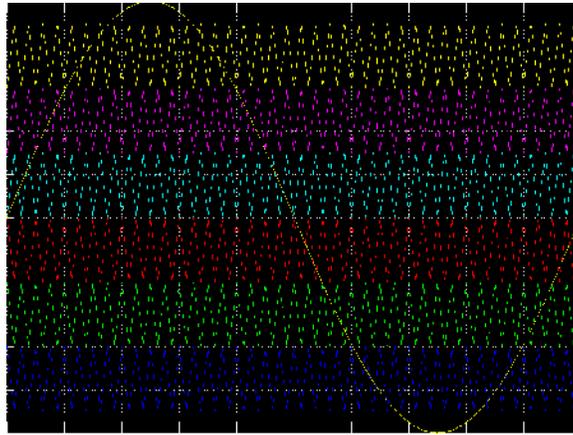


Fig. 4. Sine Pulse width modulation for seven level inverter.

**III. RESULT**

The direct current obtained by 36 cell PV modal converted into ac wave. In five level multi inverter five level of output voltage obtained. As level increases to seven level seven different output voltage obtained.

As the level increases the total harmonic distortion reduces. The simulation result of five and seven level shown in Fig. 5 & 6.

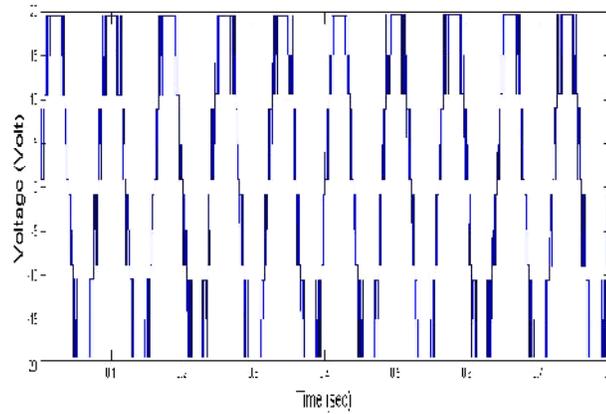


Fig. 5. Simulation result of five level Neutral point Clamped Multi Level Inverter.

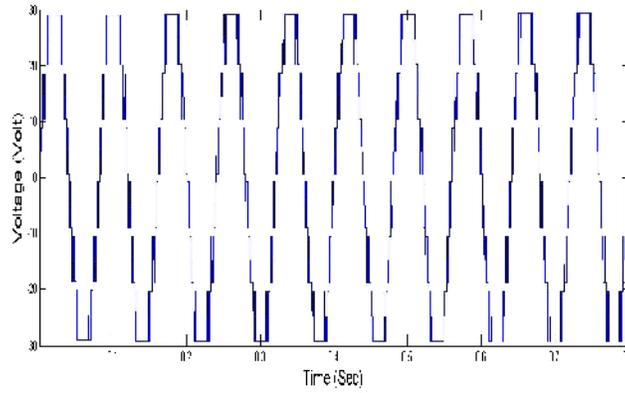


Fig. 6. Simulation result of seven Neutral point level Clamped Multi Level Inverter

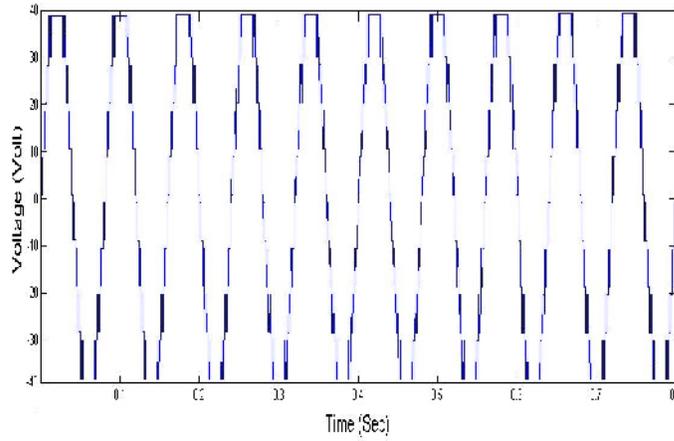


Fig. 7. Simulation result of Nine level Neutral point Clamped Multi Level Inverter.

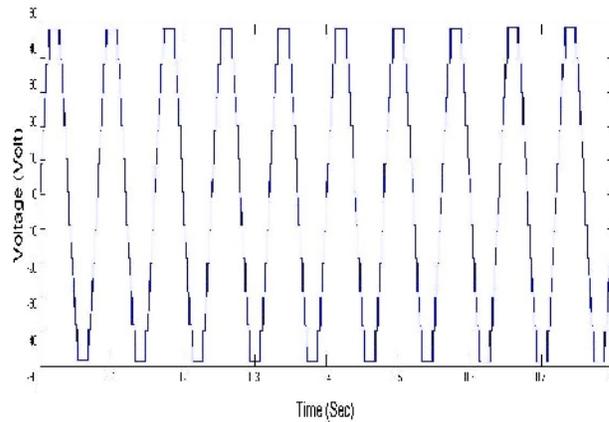


Fig. 8. Simulation result of eleven level Neutral point Clamped Multi Level Inverter.

#### IV. CONCLUSION

In this paper simulation of five, seven, nine and eleven level inverter is presented. The 36 cell solar module is connected to the multilevel inverter, the output of which is converted into stepped ac waveform. It can

also be seen from the above results that as level is increasing the sinusoidal wave becomes more pure. Distortion becomes very less. The graph shows the distortion level in different level of NPCMIL.

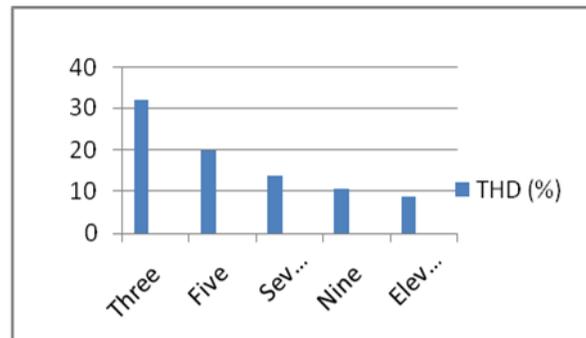


Fig. 9.

#### REFERENCES

- [1]. C. Hochgraf, R. Lasseter, D. Divan, and T. A. Lipo, "Comparison of multilevel inverters for static var compensation," *IEEE/IAS Annual Meeting*, pp.921-928, 1994.
- [2]. F.Z Peng and J. S. hi, "A Static Var Generator Using a Staircase Waveform Multilevel Voltage-Source Converter," USA Official Proceedings of the Seventh International Power Quality Conference, Sept. 17-22, 1994, Dallas/FT. Worth, Texas. pp.58-66.
- [3]. F.Z Peng, J. S. Lai, J. McKeever, and JVancoevering, "A Multilevel Voltage-Source Converter System with Balanced DC Voltages," *IEEEPESC 1995*, Atlanta, Georgia, USA, pp. 1 144-1 150.
- [4 ]. Gobinath.K, Mahendran.S, Gnanambal.I, New cascaded h-bridge multilevel inverter with improved efficiency" *International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering* April 2013
- [5]. Hava, A.M. Un, E., "Performance Analysis of Reduced Common-Mode Voltage PWM Methods and Comparison With Standard PWM Methods for Three-Phase Voltage-Source Inverters *Power Electronics*", *IEEE Transactions on* (Volume: 24 , Issue: 1 ) Jan. 2009.
- [6]. José Rodríguez, Jih-Sheng Lai, and Fang Zheng Peng, "Multilevel Inverters: A Survey of Topologies, Controls, and Applications" *IEEE Transactions On Industrial Electronics*, Vol. 49, No. 4, August 2002
- [7]. Menzies, P. Steimer, and J. K. Steike, "Five Level GTO Inverters for Large Induction Motor Drives," *IEEE/IAS Annual Meeting*, 1993.
- [8]. Sérgio Daher, Jürgen Schmid, and Fernando L. M. Antunes, "Multilevel Inverter Topologies for Stand-Alone PV Systems", *IEEE Transactions On Industrial Electronics*, Vol. 55, No. 7, July 2008.
- [9]. T. A. Meynard, H. Foch, "Multi-Level Conversion: High Voltage Choppers and Voltage-Source Inverters." *IEEE Power Electronics Specialists Conference*, 1992, pp. 397-403
- [10]. . Zhong Du, Leon M. Tolbert, Burak Ozpineci, and John N. Chiasson, "Fundamental Frequency Switching Strategies of a Seven-Level Hybrid Cascaded H-Bridge Multilevel Inverter" *IEEE Transactions On Power Electronics*, Vol. 24, No. 1, January 2009.
- [11]. Zhong Du, Burak Ozpineci, Leon M. Tolbert, and John N. Chiasson, "DC-AC Cascaded H-Bridge Multilevel Boost Inverter With No Inductors for Electric/Hybrid Electric Vehicle Applications", *IEEE Transactions On Industry Applications*, Vol. 45, No. 3, May/June 2009.
- [12]. Zhong Du ; Oak Ridge Nat. Lab., Knoxville, TN Ozpineci, B. ; Tolbert, L.M. ; Chiasson, J.N.: "DC-AC Cascaded H-Bridge Multilevel Boost Inverter With No Inductors for Electric/Hybrid Electric Vehicle Applications" *Industry Applications, IEEE Transactions on* Volume:45, Issue: 3 May-june 2009